CMOS 8-STAGE BINARY COUNTER

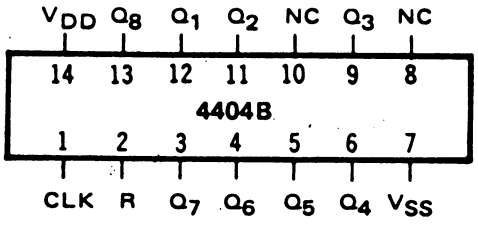
FEATURES

- 8-Stage Synchronous Counter
- Buffered Outputs from all 8 Stages
- Direct Reset
- Fully Static Operation – DC to 8MHz @ 10Vdc

DESCRIPTION

The 4404B consists of eight synchronous, single-phase clocked counting stages, with the Q output of each stage accessible. The counter is reset to all "zeroes" by a high level on the Reset line. Each stage of the counter utilizes a master-slave flip-flop configuration. The state of the counter is advanced one step in binary order on the negative-going transition of the input clock pulse.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 14-pin Cerdip

E 14-pin Epoxy

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐‾	0	No Change
‾⌐	0	Advance to next state
X	1	All Outputs are low

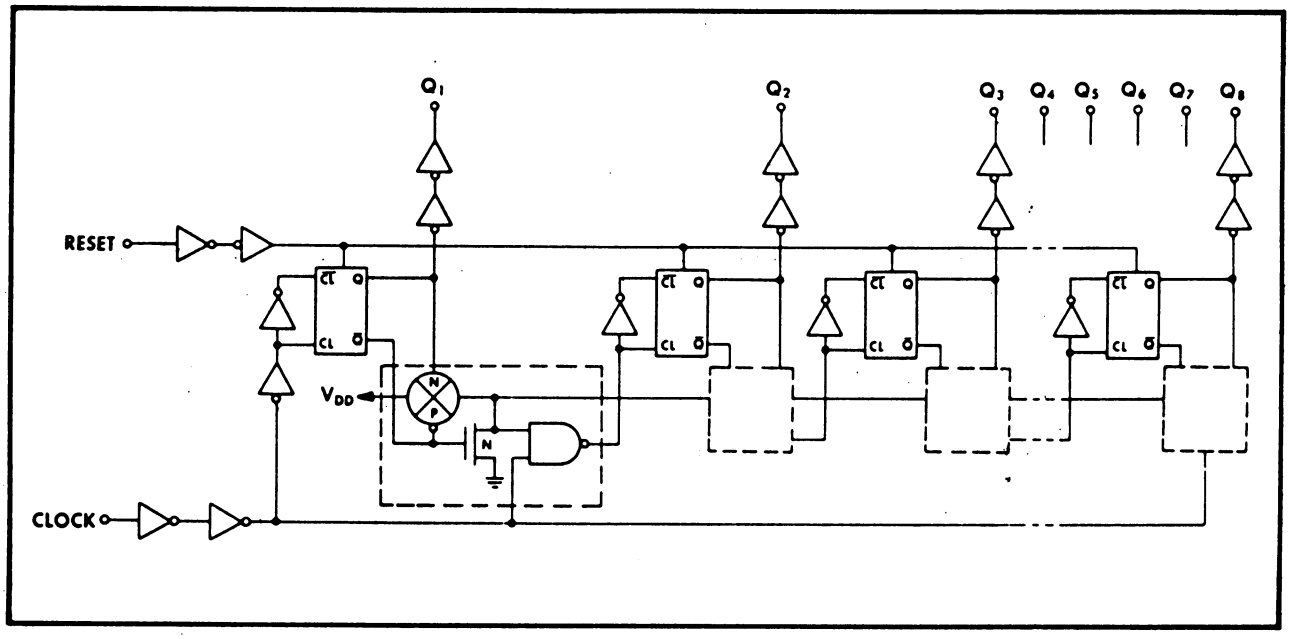
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

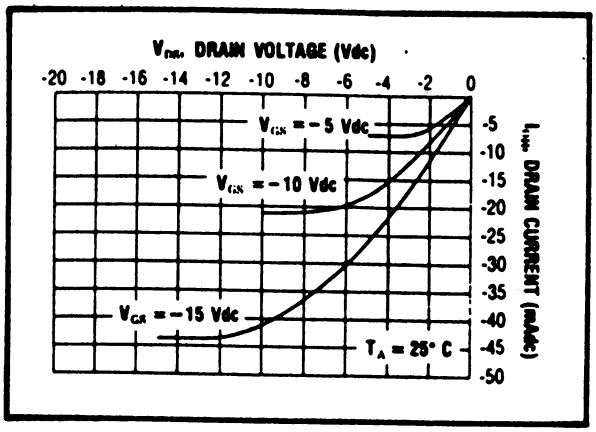
STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [3]		+25°C			T_{HIGH} [3]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	

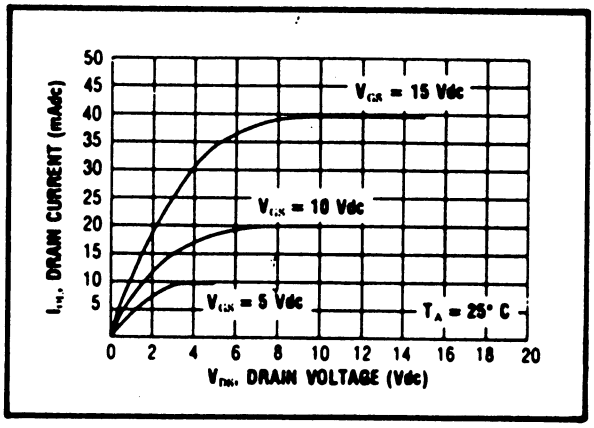
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	125	250	ns
		10	–	65	130	
		15	–	50	100	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2.0	4.0	–	MHz
		10	4.0	8.0	–	
		15	5	10	–	
MAXIMUM CLOCK RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	5	–	–	
		15	3	–	–	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	175	350	ns
		10	–	75	150	
		15	–	60	120	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
RESET REMOVAL TIME	t_{rem}	5	–	200	400	ns
		10	–	90	180	
		15	–	65	130	



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics